Comp E 475

Microprocessors

Lab 4

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# Task Description

* you have inputs**:**
  + **instruction**, 32 bits
  + **clk**
* outputs:
  + **instr\_type**, 2 bits, values from 0 to 3
    - 1 if given 32 bit instruction is Data Processing instruction
    - 2 if it's memory type instruction
    - 3 if it's branch instruction
    - 0 if not identifiable
  + **data\_instr\_type**, 3 bits, values from 0 to 4
    - 1 if given Data Processing instruction is "Immediate" type
    - 2 if it's "Register shifted by value" type
    - 3 if it's "Register shifted by register" type
    - 4 if it's "Multiplication" type
    - 0 if not identifiable

# Solution

In order to solve the problem, I used if and case statements. The code is small and simple and self-explanatory.

The code :

`timescale 1ns / 1ps

module HW3

output reg [1:0] ins\_type,

input [31:0] ins,

output reg [2:0] d\_type

);

always @(\*) begin

case(ins[27:26])

00: begin

ins\_type = 2'b01;

d\_type = ins[25] ? 3'b001 :

!ins[25] && !ins[4] ? 3'b010 :

ins[25] && ins[7] && ins [4] ? 3'b011 :

!ins[25] && !ins[24] && !ins[7] &&

ins[6] && ins[5] && !ins[4] ? 3'b100 : 3'b000;

end

01: ins\_type=2'b10;

10: ins\_type=2'b11;

default: ins\_type=2'b00;

endcase

end

endmodule

# Simulation & Verification

# Comparison

Was a bit harder than previous labs because we got introduced to git.

# Conclusion